ANGSEMI

Datasheet

Magnetic Sensor ICs

Digital Linear Hall Sensor With Programmable Switch

AS1560

General Description

AS1560 is a low-power digital linear Hall sensor in measuring the intensity of the magnetic flux through selecting options of the various sensitivity with the low power consumption providing a built-in 16 bits ADC digital output. It can also detect the open/close state for many applications by one or multiple external magnets.

This sensor is comprised of a Hall element, an offset cancellation circuitry, a programmable gain amplifier, a 16-bits low power ADC, and control logic in a single chip. The adjustment of the open/close state threshold values, the magnetic polarity, and the operation period can be programmed through I2C interface. The software package supports to convert the magnetic strength into the angle or distance by detecting intensity of flux between the external magnet and the sensing element. Because the small WLCSP package, the low current consumption, and the stable performance, the device can be used in the hand set and consumer electronics and any other industries. One of the typical applications in the smart phone is the lid opening angle measurement system.

A key feature of the device is its Programmable Hall switch, which allows users to define the comparison range via the comparison register through I²C. Additionally, the output logic can be configured to toggle between high and low states when the detected magnetic field meets the preset threshold.

The device is a RoHs and Green compliant DFN2020-6L package.

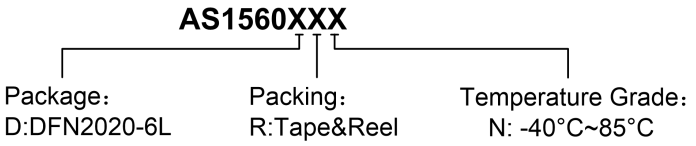
Features

- Programmable Magnetic Threshold Switching with Customizable BOP/BRP Setting Hall Switch
- Supply Voltage Range V_{DD}: 1.7V to 3.6V
- Operation Current:
  - ✓ 26uA (typ.) at 50Hz Operating Frequency AVER_Z=0x20
  - ✓ 260uA (typ.) at 500Hz Operating Frequency AVER_Z=0x20
- Built-in ADC for magnetometer data outputs
- 16-bits Data Output for each built-in Hall Sensor
- Configurable magnetic sensitivity level and measurable range for example:
  - ✓ Maximum Dynamic Range: -163.84mT ~ +163.84mT, 5.0uT/LSB
- High Resolution:
  - ✓ High sensitivity: 1.25uT/LSB with 40.96mT Dynamic Range
- INTB pin Real Time Event Notification
- Built-in Magnetic Sensitivity Adjustment Circuit
- Programmable Through I²C Bus Compatible Fast Mode up to 1MHz
- Up to 4KHz High Speed Data Output Rate
- Five Addresses Via an External Resistor.
- Operation Mode:
  - ✓ Power Down
  - ✓ Single Measurement
  - ✓ Continuous Measurement
- Low Power Design: Standby Mode 1.3uA
- Built-in Oscillator for internal Clock Source
- Power On Reset
- RoHS and Green Compliant
- Small DFN2020-6L Packages
- -40℃ to +85 ℃ Temperature Range

Applications

- Magnetometer for External Detection
- Lid Opening Angle Detection
- Mobile Phones and Smart Phones
- Touch Screen Disable
- Mechanical Switch Replacement
- Universal Remote Control
- Control Display Switch
- VCM Modules

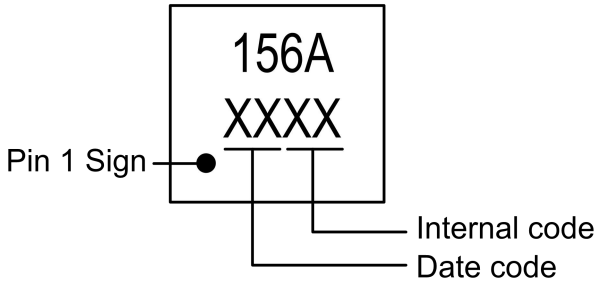
Ordering Information



Part Number	Resolution	Package Type	Package Qty	Temperature	Eco Plan
AS1560DRN	16-bits	DFN2020-6L	7-in reel 3000pcs/reel	-40～85℃	Green

Marking Information

DFN2020-6L



Typical Application Circuit

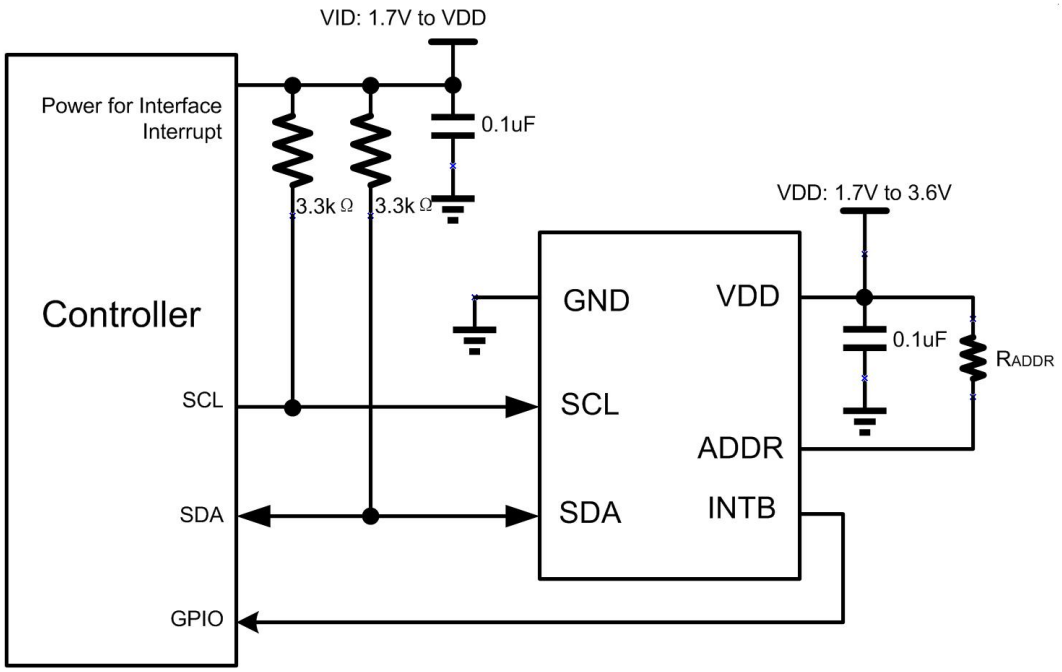


Figure 1, Typical I2C Mode Application Circuit of AS1560

Address = 0x1A: R_{ADDR} ≥ 500KΩ or Remove R_{ADDR} connected to GND;

Address = 0x1B: R_{ADDR} = 104KΩ ±10%;

Address = 0x1C: R_{ADDR} = 40KΩ ±10%;

Address = 0x1D: R_{ADDR} = 15KΩ ±10%;

Address = 0x1E: R_{ADDR} ≤ 5KΩ or Remove R_{ADDR} connected to VDD.

Pin Configuration

DFN2020-6L (Top View):

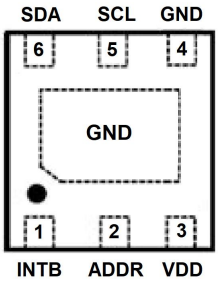


Figure 2, Pin Assignments of AS1560

Pin Name	Pin No. DFN2020-6L	I/O	Pin Function
1	INTB	O	Interrupt Output Pin. Magnetic Switch Activation and Data-ready Alerts.
2	ADDR	I	Address Selector. Refer to Figure 1.
3	VDD	P	Input Power Supply.
4	GND	P	Ground.
5	SCL	I	I2C interface clock signal pin.
6	SDA	I/O	I2C interface data signal pin. Output: Open-Drain and Push-Pull.
EP	EXPAD	-	Connected to GND.

Block Diagram

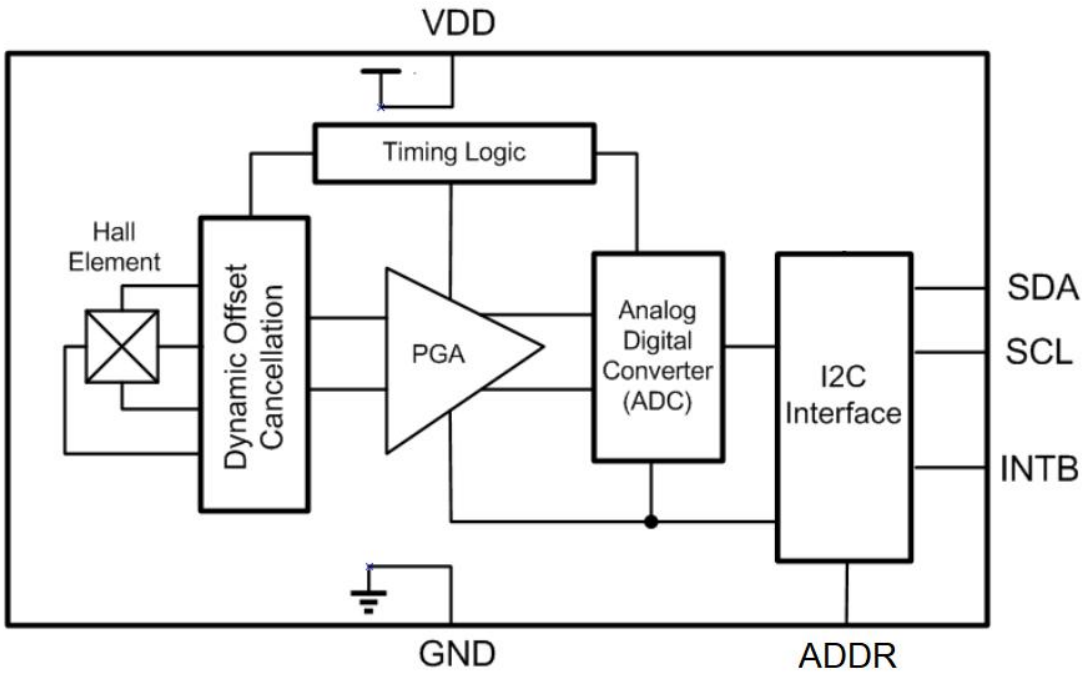


Figure 3, Block Diagram of AS1560

Absolute Maximum Ratings[1] (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Unit
VDD, SCL, SDA, ADDR and INTB Pins to GND	V*	-0.3 to +4.0	V
Input Current	I_{IN}	-10 to +10	mA
ESD	HBM	2000	V
Power Dissipation	P_D	0.54	W
Storage Temperature Range	T_S	-40 to +85	℃
Operating Junction Temperature Range	T_J	-40 to +125	℃

● Recommended Operating Conditions[2]

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	+1.7 to +3.6	V
Operating Temperature Range	T_{OP}	-40 to +85	℃

Note: 1: Stresses above those listed in absolute maximum ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one absolute maximum rating should be applied at any one time.
Note 2: The device is not guaranteed to function outside of its operating conditions.

● Electrical Characteristics

(T_A = -40 to +85℃ unless otherwise noted. Typical values are at T_A = +25℃, V_{DD} = 3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Supply Voltage		1.7	3.3	3.6	V
I_Q	Quiescent Supply Current	AVER_Z=0x20, 5Hz Sampling	-	1.3	-	uA
		AVER_Z=0x20, 50Hz Sampling	-	26	-	uA
		AVER_Z=0x20, 500Hz Sampling	-	260	-	uA
		AVER_Z=0x10, 500Hz Sampling	-	160	-	uA
		AVER_Z=0x30, 500Hz Sampling	-	460	-	uA
		AVER_Z=0x40, 500Hz Sampling	-	850	-	uA
		AVER_Z=0x50, 500Hz Sampling	-	1650	-	uA
I_{SUP}	Suspend Current	Standby Mode	-	1.3	-	uA
T_{TURNON}	Supply Turn-On Time (note 3)	Time for V_{DD} to reach $V_{DD(MIN.)}$	-	-	1.0	mS
$T_{RESTART}$	Re-start Time (note 3)		-	-	10.0	mS
T_{OFF}	Turn-Off Time		30	-	-	mS
Output Characteristics						
ODR	Maximum Output Data Rate		-	4.0	-	KHz
D_{BIT}	Measurement data output bit		-	16	-	bit
DR	Dynamic Range	DR & RES=0x00	-	±163.84	-	mT
		DR & RES=0x20	-	±81.92	-	mT
		DR & RES=0x40	-	±40.96	-	mT
RES	Resolution	DR=±163.84mT	-	5.0	-	uT/LSB
		DR=±81.92mT	-	2.5	-	uT/LSB
		DR=±40.96mT	-	1.25	-	uT/LSB
BOF	Magnetic Sensor Initial Offset	DR=±40.96mT	-1000	-	+1000	LSB
R_{LSB}	LSB Range	16-bit	-	65536	-	LSB
SENDR	Sensitivity Drift	DR=±40.96mT	-	400	-	PPM/℃
BOFDR	Offset Drift	DR=±40.96mT	-	5.0	-	uT/℃
LIN	Linearity	T_A = +25℃	-	±0.5	-	%
SDA, SCL and INTB Specifications						
V_{INL}	Input Low Threshold Voltage		0	-	0.3*V_{DD}	V
V_{INH}	Input High Threshold Voltage		0.7*V_{DD}	-	V_{DD}	V
V_{OL}	SDA pin Output Voltage		-	-	0.3*V_{DD}	V
V_{OH}	High Level Output Voltage		0.7*V_{DD}	-	V_{DD}	V

Note 3: Sequence of power activation is described in Figure 4.
Note 4: After VDD(MIN) is reached, user must wait for at least 10mS.
Note 5: When the applied magnetic filed goes over under B_{SX}, the magnetic does not move up to the mechanical endpoints in either detection mode (X indicates sensitivity mode such as 1, 2 and 3).
Note 6: Value of measurement data register on shipment test without applying magnetic field on purpose.
Note 7: V_{OH} Output is Push-Pull, V_{OL} Output is open-drain and Push-Pull. Connect a pull-up resistor externally is open-drain mode.

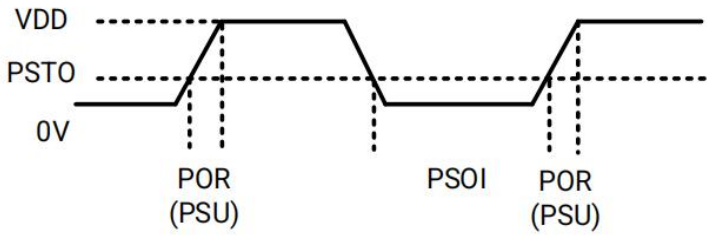


Figure 4, VDD Power Sequence of AS1560

PSTO: Power Supply Turn Off Voltage	PSTO: Max.=0.1V
PSOI: Power Supply Turn Off Interval	PSOI: Min.=30mS
POR: Power On Reset	POR: Max.=10mS
PSU: Power Supply Rise Time	PSU: Max. =1mS

When the POR circuit detects an increase in VDD value, it resets all internal circuits and initializes all registers. After being reset, the device transits to Standby Mode.

■ Hall Sensor Location

The Fig 5 is hall sensor location, where marks the IC number.

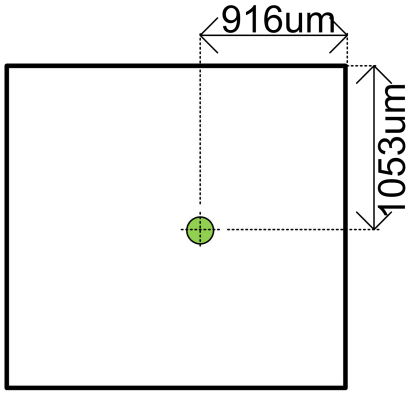


Fig 5, Hall Sensor Location and Magnetic Field Direction

● I³C Bus Interface Electrical Characteristics

I2C Mode:

f_{SCL}<=400KHz, unless otherwise specified.

Table 1, Serial Interface Characteristics at Fast Mode

AS1560 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I2C Compatible Voltage Specifications (SCL, SDA)						
V_{IL}	Low Level Threshold Voltage (note 8)		0	-	0.3*V_{DD}	V
V_{IH}	High Level Threshold Voltage (note 8)		0.7*V_{DD}	-	V_{DD}	V
I2C Compatible Timing Specifications (SCL, SDA)[4], see Figure 5						
f_{SCL}	SCL clock frequency	Standard Mode	-	-	100	kHz
		Fast Mode	-	-	400	kHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7	-	-	uS
		Fast Mode	1.3	-	-	uS
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0	-	-	uS
		Fast Mode	0.6	-	-	uS
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	-	-	uS
		Fast Mode	1.3	-	-	uS
$t_{HD,STA}$	Hold time for a repeated START condition	Standard Mode	4.0	-	-	uS
		Fast Mode	0.6	-	-	uS
$t_{SU,STA}$	Setup time for a repeated START condition	Standard Mode	4.7	-	-	uS
		Fast Mode	0.60	-	-	uS
$t_{SU,DAT}$	Data Setup time	Standard Mode	0.25	-	-	uS
		Fast Mode	0.10	-	-	uS
$t_{HD,DAT}$	Data hold time	Standard Mode	0.05	-	3.45	uS
		Fast Mode	0	-	-	uS
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0	-	-	uS
		Fast Mode	0.6	-	-	uS
t_{SP}	Pulse width of spike which must be suppressed by the input filter	Standard Mode	-	-	50	nS
		Fast Mode	-	-	50	nS
t_{RCL}	Rise time of SCL signal (note 8)	Standard Mode	-	-	1000	nS
		Fast Mode	20	-	300	nS
t_{FCL}	Fall time of SCL signal (note 8)	Standard Mode	-	-	300	nS
		Fast Mode	20*V_{DD}/3.6	-	300	nS
t_{RDA}	Rise time of SDA signal (note 8)	Standard Mode	-	-	1000	nS
		Fast Mode	20	-	300	nS
t_{FDA}	Fall time of SDA signal (note 8)	Standard Mode	-	-	250	nS
		Fast Mode	20*V_{DD}/3.6	-	250	nS

Note 8: These parameters do not comply with I2C requirements.

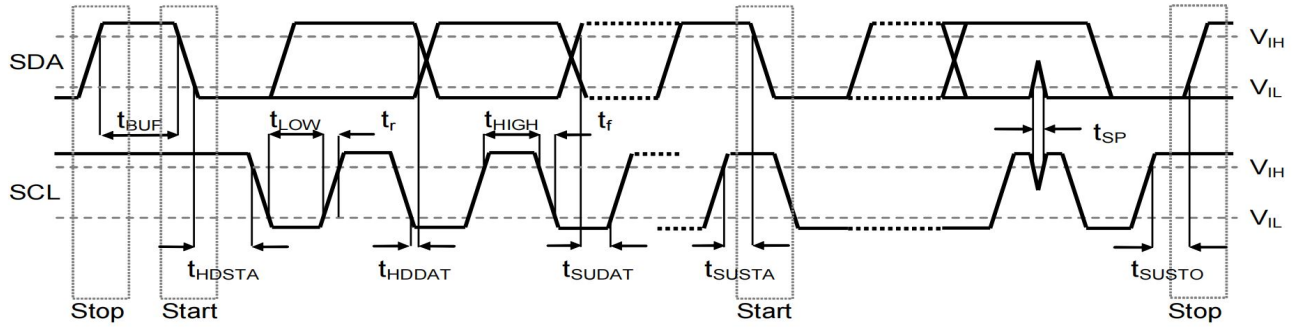


Figure 5, Serial Interface Timing for F/H-Speed-Mode I2C

Function Description:

AS1560 is a low-power digital linear Hall sensor in measuring the intensity of the magnetic flux through selecting options of the various sensitivity with the low power consumption providing a built-in 16 bits ADC digital output. It can also detect the open/close state for many applications by one or multiple external magnets.

This sensor is comprised of a Hall element, an offset cancellation circuitry, a programmable gain amplifier, a 16-bits low power ADC, and control logic in a single chip. The adjustment of the open/close state threshold values, the magnetic polarity, and the operation period can be programmed through I2C interface. The software package supports to convert the magnetic strength into the angle or distance by detecting intensity of flux between the external magnet and the sensing element. Because the small WLCSP package, the low current consumption, and the stable performance, the device can be used in the hand set and consumer electronics and any other industries. One of the typical applications in the smart phone is the lid opening angle measurement system.

A key feature of the device is its Programmable Hall switch, which allows users to define the comparison range via the comparison register through I²C. Additionally, the output logic can be configured to toggle between high and low states when the detected magnetic field meets the preset threshold.

Operation Modes:

AS1560 has the following four operation modes:

(1) Stand-by mode

(2) Single measurement mode

(3) Continuous measurement mode

When power is turned on, AS1560 is in stand-by mode. When a specified value is set to HSSON, AS1560 transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 30mS(Twat) is needed before setting another mode.

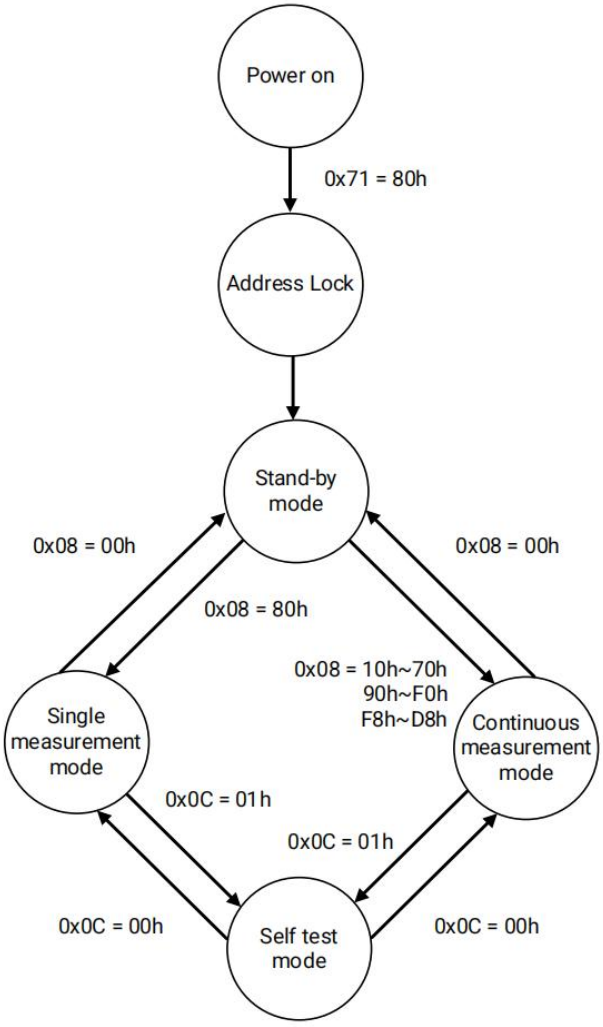


Figure 6, Operation Mode

Address Lock:

When the IC is powered on, the address is configured by external resistors based on their resistance values. To lock the address, write **0x80h** to register **0x71h**. The locked address remains fixed despite environmental variations and persists until a power cycle resets it.

Stand-by Mode

The default mode after Address Lock is **Standby Mode (0x08 = 80h)**. In this mode, all internal circuits are deactivated, except for the oscillator and regulator, to minimize power consumption. Users retain full access to all registers during Standby Mode, and the state of data within the Read/Write registers is preserved. Registers can be reset using a soft reset command.

Single Measurement Mode:

In **Single Measurement Mode**, the device records measured data in the data registers. Following the recording, the device automatically reverts to Standby Mode. The transition reset the CNTL1 [7:4] bits = "0000", and the Data Ready (DRDY) bit in the STAT1 register is set to "1", indicating that the **data is ready** to be read. Upon reading any of the measurement data registers, the DRDY bit resets to "0". To initiate another measurement, users must manually set CNTL1 [7:4] bits = "1000".

Continuous Measurement Modes:

In **Continuous Measurement Mode**, the AS1560 performs measurements at preset frequencies continuously. Measured data is stored in the Output Data Registers. Each subsequent measurement cycle automatically begins at the designated time, updating the Output Data Registers with new data.

Normal Read Sequence:

(1) Read STAT1register:

- **Polling STAT1 register**: Continuously check the STAT1 register until it indicates data readiness.
- **DRDY(Data Read) Bit**: shows if the hall sensor data is ready or not
  0: no data ready
  1: data ready
- **DOR(Data Overrun) Bit**: Indicates if any data was skipped before the current data in Continuous Measurement Mode.
  0: no skipped data
  1: data skipped.

(2) Read Measurement Data:

- Data Range: Read register range from 0x11h - 0x12h for Z-axis data, which spans from -32767 to 32767 LSB.

- Data Read Process: When the reading process begins, both the DRDY and DOR bits are reset to 0.

● Programmable Hall Switch:

Limitations of Common Hall Switches:

Common Hall switches are typically configured with fixed triggering magnetic field thresholds (BOPs, BRPs) and a fixed hysteresis to counteract environmental noise. These switches activate only when the magnetic field strength exceeds a lower limit, lacking the capability to verify the authenticity of the approached magnetic field.

Advantages:

The AS1560 stands out with its programmable Hall switch functionality, allowing for the customization of both the high and low BOP/BRP within a broad operational range of ±160 mT. This adaptability extends to setting the required hysteresis to better manage ambient noise, thereby enhancing measurement accuracy and reliability.

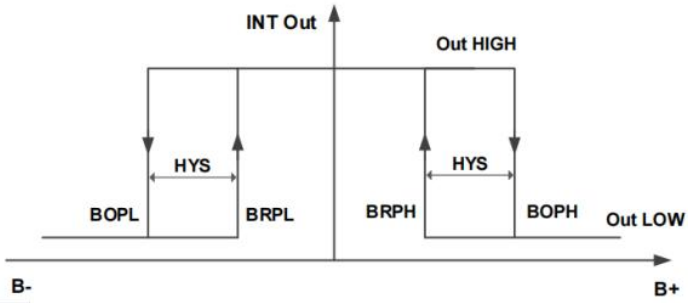


Figure 7A, Trigger Conditions of Magnetic Operation Characteristic (INT_TYP=0)

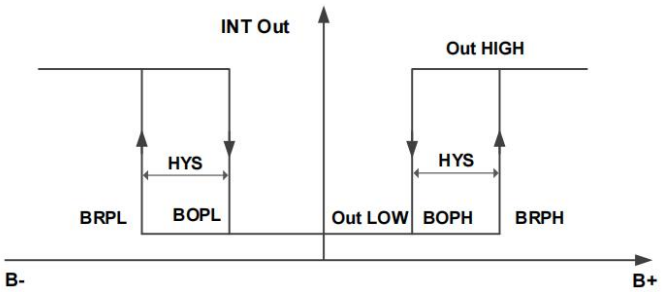


Figure 7B, Trigger Conditions of Magnetic Operation Characteristic (INT_TYP=1)

The AS1560 supports configurable interrupt trigger modes to accommodate various application requirements (see Figure 1). These modes are controlled through Register 0x01 (INT_Condition) and determine when the INTB pin is pulled low:

- INT_TYP=1: INTB is active (Low) when the magnetic field is within the selected BOPL/BOPH values (i.e., BOPL < Bapplied < BOPH) .

- **INT_TYP=0**: INTB is active (Low) when the magnetic field is outside of the selected BOPL/BOPH values (i.e., Bapplied < BOPL || Bapplied > BOPH) .

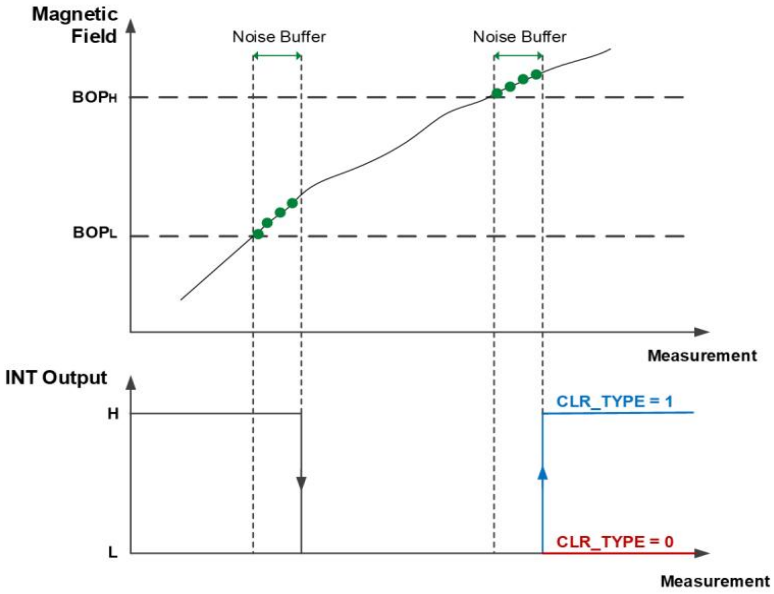


Figure 8, INTB Delay with n-Point Trigger Filter (Example: n=4)

Enhanced Interrupt Management with Noise Buffers:

The device includes features designed to maintain interrupt stability in noisy environments. By configuring the interrupt behavior through dedicated registers, the sensor can suppress false triggers and maintain accurate event detection.

- **Register 0x00 (INT_DELAY):** Sets the number of consecutive threshold events (n) required before INTB is asserted. This filter helps to reject single-sample noise spikes and ensures that only sustained magnetic changes trigger an interrupt.

- **Register 0x01 (INT_CONFIG):** Controls how INTB behaves after being triggered.

  − Interrupt_Lock = 0 (Latch mode): INTB remains low after the interrupt condition is met and must be cleared manually using Interrupt_Unlock.

  − Interrupt_Lock = 1 (Normal mode): INTB automatically returns high when the magnetic field falls below release point (BRP).

Reset Functions

AS1560 has setting, stand-by and measurement mode. User can choose arbitrary mode thorough the I2C interface. Power On Reset (POR) works until VDD reaches to the operation effective voltage on power-on sequence. After POR is completed, all registers are initialized and AS1560 transits to Power-down mode.

AS1560 has two types of reset:

(1) , Power On Reset (POR): When V_{DD} rise is detected, POR circuit operates, an AS1560 is reset.

(2) , Soft Reset: AS1560 is reset by setting register **SRST bit**.

After reset is completed, all registers and FIFO buffer are initialized and AS1560 transit to Power-down mode automatically.

Digital Interface and Registers

I2C Serial Interface Description:

The AS1560 supports the I2C compatible interface and the data transmission protocol in two modes: standard mode and the fast mode. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master, the devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The AS1560 operates as a slave on the I2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

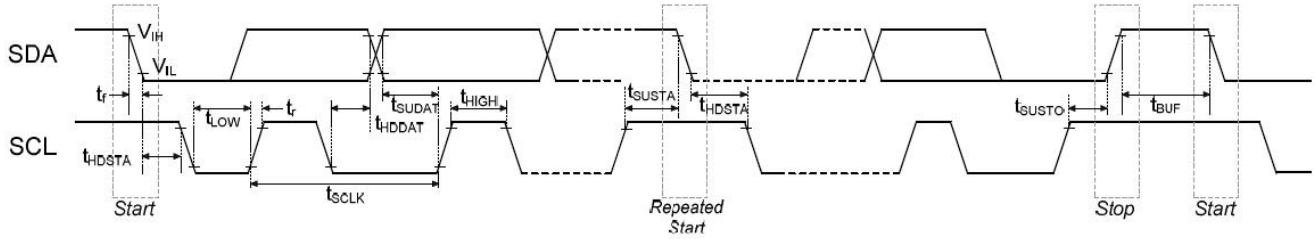


Figure 9, Serial Interface Timing for F/S-Mode I2C

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals. Accordingly, the following bus conditions have been defined:

Bus Not Busy:

Both data and clock lines remain High.

Start Data Transfer:

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines a START condition.

Stop Data Transfer:

A change in the state of the data line, from LOW to HIGH, while the clock is HIGH defines a STOP condition.

Data Valid:

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth-bit. Within the I2C bus specifications, a standard mode (100kHz clock rate), a fast mode (400kHz clock rate) and high speed mode (up to 3.4Mbps in write mode) are defined. The AS1560 works in the two modes.

Acknowledge:

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data. The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked. AS1560 generates an acknowledge after reception of a start condition and slave address.

When a WRITE instruction is executed, AS1560 generates a acknowledge after all bytes are received. When a READ instruction is executed, AS1560 generates an acknowledge then transfers the data stored at the specified address. Next, AS1560 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AS1560 transmits the 8bit data stored at the next address. If no acknowledge is generated, AS1560 stops data transmission. Each receiving device, when accessed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

Slave Address Byte:

The address byte is the first byte received following the START condition from the master device. The 7-bit slave address ranging from 0x18h to 0x1Fh. When using an 8-bit address format, the 7-bit address (0x18h to 0x1Fh) is shifted to the left by one bit (Bit 7:1), and bit 0 is set to 0.

Serial Data-Words	Slave Address Byte (0x48h)							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Function	0	0	1	1	SAD2	SAD1	SAD0	R/W

Table 2, Address Byte Code

RADDR	SAD2	SAD1	SAD0	Slave Address（7-bit）	Slave Address（8-bit）	AS1560
Refer to Figure 1	0	1	0	1AH (0011010R/W)	34H (0011010R/W)	Default
	0	1	1	1BH (0011011R/W)	36H (0011011R/W)	●
	1	0	0	1CH (0011100R/W)	38H (0011100R/W)	●
	1	0	1	1DH (0011101R/W)	3AH (0011101R/W)	●
	1	1	1	1EH (0011111R/W)	3CH (0011111R/W)	●

Table 3: Slave Address Setting Table

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.

When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge, and then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

Write Instruction: Slave Receiver Mode (Write Mode):

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

When the R/W bit is set to "0", AS1560 performs write operation. In write operation, AS1560 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

Serial Data Bits	MSB							LSB
Input Register	A7	A6	A5	A4	A3	A2	A1	A0

After receiving the second byte (register address), AS1560 generates an acknowledge then receives the third byte. The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AS1560 generates an acknowledge after all bytes are received. Data transfer always stops with a stop condition generated by the master.

Serial Data Bits	MSB							LSB
Input Register	D7	D6	D5	D4	D3	D2	D1	D0

AS1560 can write multiple bytes of data at a time. After reception of the third byte (control data), AS1560 generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address. Actual data is written only to Read/Write registers.

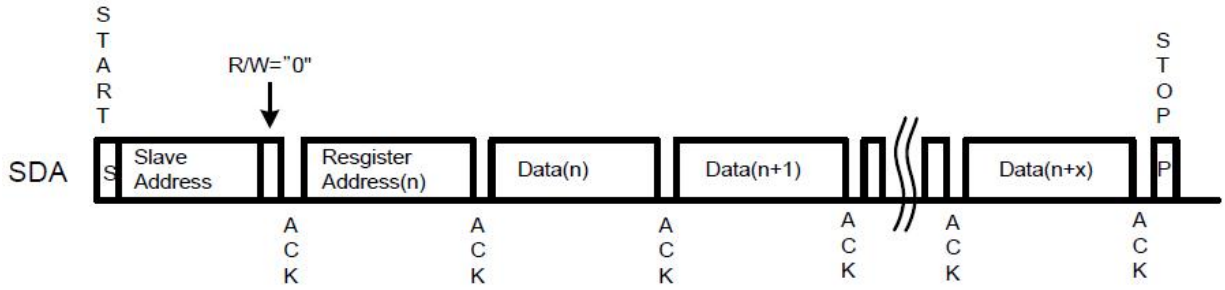


Figure 10, Write Command for F/S-Mode I2C

Read Instruction: Slave Transmitter Mode (Read Mode):

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition.

Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

When the R/W bit is set to "1", AS1560 performs read operation. If a master IC generates an acknowledge instead of a stop condition after AS1560 transfers the data at a specified address, the data at the next address can be read.

One or Multiple Byte READ:

By multiple byte read operation, data at an arbitrary address can be read. The multiple byte read operation requires executing WRITE instruction as dummy before a slave address for the READ instruction (R/W bit="1") is transmitted. In random read operation, a start condition is first generated, then a slave address for the WRITE instruction (R/W bit="0") and a read address are transmitted sequentially. After AS1560 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit="1") are generated again. AS1560 generates an acknowledge in response to this slave address transmission. Next, AS1560 transfers the data at a specified address, and then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

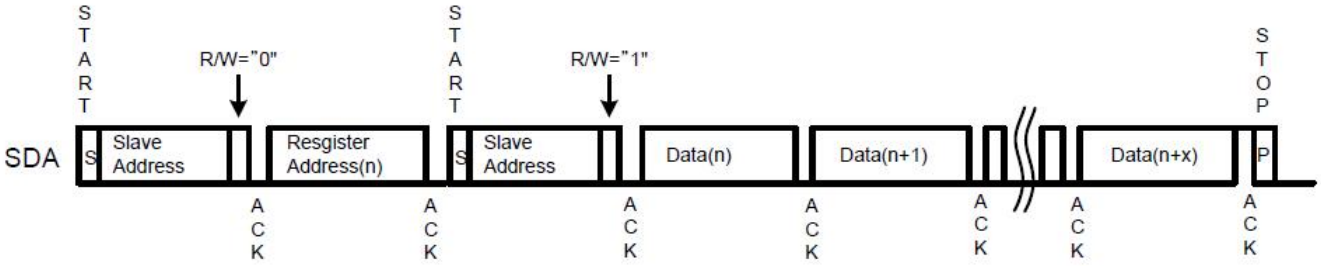


Figure 11, Multiple-Byte data Read Command for F/S-Mode I2C

Appendix I3C Serial Interface

I3C Serial Interface Description:

The I3C bus interface of AS1560 supports the I2C mode (400KHz max.) and the I3C single data rate (SDR) mode (12.5MHz max.).

Table 4, Bus Protocol Configuration:

Protocol	Bit Length	Description	Abbreviation
START Condition	-	Input at the start of communication	S
Slave Address	7	Select Slave Device	-
Read/Write Control Bit	1	0: Write 1: Read	R/W
Register Address	8	Set Access Address	-
Control Data	8	Write/Read Data	-
Repeated START	-	Two or more instance of a START in a row without an intervening STOP	Sr
STOP Condition	-	Input at the end of communication	P
Acknowledge	-	Generated when receiving data	ACK
Transition Bit	-	Generated when sending data	T
Parity Bit	-	Received when writing data	PAR
HDR Exit Pattern	-	Entered when returning from error condition	-

Start Condition and Stop Condition:

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a START condition is generated. Every instruction starts with a START condition.

If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a STOP condition is generated. Every instruction stops with a STOP condition.

The I3C START and STOP are identical to the I2C START and STOP in their signaling, but they may vary from I2C in their timing. Refer to ***I2C Mode*** and ***I3C Mode Description***.

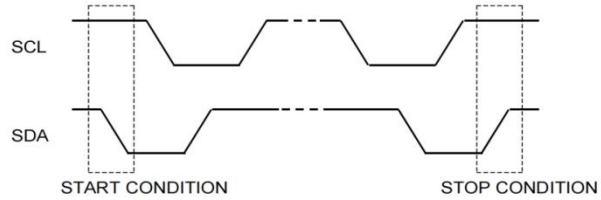


Figure 12, Start and Stop Conditions

Acknowledge:

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred to acknowledge. With this operation, whether data has been transferred successfully can be checked.

In I2C mode, AS1560 generates an acknowledge after reception of the START condition and Slave Address. When a WRITE instruction is executed, AS1560 generates an acknowledge (without Handoff) after every byte is received. When a READ instruction is executed, AS1560 generates an acknowledge (without Handoff) then transfers the data stored at the specified address. Next, AS1560 releases the SDA line then monitors the SDA line. If a Master IC generates an acknowledge instead of the STOP condition, AS1560 transmits the 8-bit data stored at the next address. If no acknowledge is generated, AS1560 stops data transmission.

AS1560 generates an acknowledge after reception of a START condition and Broadcast Address **(7’0x7Eh)**. When a WRITE instruction is executed, AS1560 generates an acknowledge (with Handoff). When a READ instruction is executed, AS1560 generates an acknowledge (without Handoff).

In I3C SDR mode, AS1560 generates an acknowledge after reception of a START condition and under following conditions.

(1) When receiving its own Dynamic Address.

(2) When a Broadcast Address is received.

(3) When a Slave Address is received by Dynamic Address Assignment.

In case of (1), when the R/W bit is set to “1”, it returns one clock (without Handoff), and when R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff).

In case of (2), when the R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff).

In case of (3), it returns an acknowledge of one clock (without Handoff).

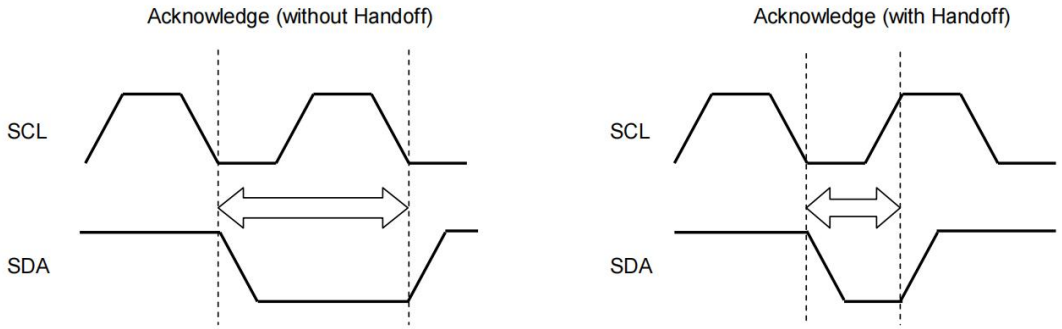


Figure 13, Generation of Acknowledge without/with Handoff

Broadcast Address

The Broadcast Address of Slave devices is **7'0x7Eh.**

All I3C Slave match Address value **7'0x7Eh**. No I2C Slave will match address **7'0x7Eh**.

MSB							LSB
1	1	1	1	1	1	0	R/W

The first byte including a Broadcast address is transmitted after the START condition, and all I3C Slaves are selected on the bus.

When a Broadcast address is transferred, all I3C Slave generate an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", write instruction is executed.

Slave Address

The Slave Address of AS1560 is **7'0x19h**

MSB							LSB
0	0	0	1	1	0	1	R/W

The first byte including a slave address is transmitted after the START condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.

When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", write instruction is executed.

This CCC Command initiates I3C communication and Dynamic Address assignment from the default I2C status to I3C SDR mode. The SETDASA CCC (= 0x87) is a flow for assigning a Dynamic Address based on the Slave Address in the I2C state. AS1560 is capable of assigning a Direct Address using Direct CCC. The Slave Address of AS1560 is 19h.

The newly assigned address is transmitted in the Dynamic Address byte shown as 0, where the 7 most significant bits (Bits [7:1]) include the 7-bit Dynamic Address and the least significant bit (Bit [0]) contains the value 1'b0. If this least significant bit (Bit [0]) is set to 1'b1, AS1560 will not accept the Dynamic Address.

Dynamic Address

In I2C mode, AS1560 is assigned a Dynamic Address by performing **SETDASA** or **ENTDAA** flow. After the flow is completed, AS1560 communicates in I3C SDR mode.

SETDATASA (Set Dynamic Address from Static Address)

The SETDASA CCC (=0x87) is a flow for assigning Dynamic Address based on the Slave Address in the I2C state. AS1560 can assign a Dynamic Address by Direct CCC. The Slave Address of AS1560 is **7'0x19h**.

The newly assigned address is transmitted in the Dynamic Address byte shown in Figure 21, where the 7 most significant bits (Bits [7:1]) contain the 7-bit Dynamic Address, and the least significant bit (Bit [0]) is filled with the value 1'b0. If this least significant bit (Bit [0]) has the value 1'b1, AS1560 will not accept the Dynamic Address.

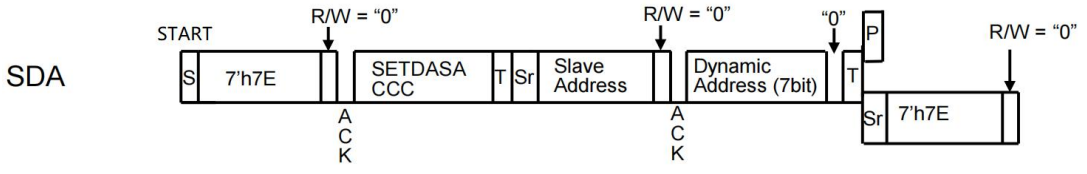


Figure 14, SETDATASA Format 1: Primary

Transition-Bit (T-Bit):

In I3C, the data words match I2C only in the sense that they are both 9 bits long.

In I2C, the ninth data bit written by the Master is an acknowledge by the Slave. By contrast, in I3C the ninth data bit written by the Master is the parity of the preceding eight data bits. In SDR terms, the ninth bit of write data is referred to as the T-Bit (for 'Transition'). The ninth data bit of each SDR data word written by the I3C Master (also referred to as the T-Bit) is a Parity bit, calculated using odd parity. Parity can help in detecting noise-caused errors on the line. The value of this parity bit shall be the XOR of the 8 data bits with 1, i.e.: **XOR(Data [7:0], 1).**

T (Parity) bit writes shall always be kept valid through the SCL high period. In the case of a T-Bit representing the last data byte, the write is therefore kept valid through the SCL high period, and the next SCL low can then be used to either change the SDA, or not change the SDA, in preparation for the Repeated START condition or STOP condition that follows. If parity is different, AS1560 will not receive data.

In I2C, the ninth data bit from Slave to Master is an acknowledge by the Master. By contrast, in I3C this bit allows the Slave to end a read and allows the Master to abort a read. In SDR terms, the ninth bit of read data is referred to as the T-Bit (for 'Transition').

If transmission of the number of bytes set by ***SETMRL*** has not been completed, AS1560 generates T-Bit = "1" and transmits data at the next address from the falling edge of SCL after that. When transmission of the number of bytes set by ***SETMRL*** is completed, AS1560 generates T-Bit = "0" and then releases the SDA line.

I3C SDR Mode:

When Dynamic Address is assigned properly, AS1560 shifts to I3C SDR mode.

I3C SDR mode is significantly similar to the I2C protocol in terms of procedures and conditions. In I3C SDR mode, AS1560 can communicate with Private Messages or Common Command Code (CCC).

Private Messages:

WRITE Instruction:

When the R/W bit is set to "0", AS1560 performs write operation.

In write operation, AS1560 generates an acknowledge (with Handoff) after receiving a START condition and the first byte (Dynamic Address). The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

After receiving the second byte (register address), AS1560 receives a T-Bit then receives the third byte.

The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AS1560 generates a T-Bit after every byte is received. Data transfer always stops with a STOP condition generated by the Master.

AS1560 can write multiple bytes of data at a time. The maximum value is determined Max Write Length.

After reception of the third byte (control data), AS1560 receives a T-Bit then receives the next data. If additional data is received instead of a STOP condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.

Actual data is written only to Read/Write registers (***Table 16 Register Table***).

Table 5, I3C Private WRITE Sequence

Master	Slave Device (AS1560)	Bus Condition
START Condition	Input at the start of communication	Open-Drain
7-bit Dynamic Address		Open-Drain
R/W="0"	ACK (with Handoff)	Open-Drain
Access Address (1 Byte)	Parity Check, using T-Bit	Push-Pull
Control Data (1 Byte)	Parity Check, using T-Bit	Push-Pull
Control Data (1 Byte)	Parity Check, using T-Bit	Push-Pull
|	|	|
STOP Condition	Input at the end of communication	Push-Pull

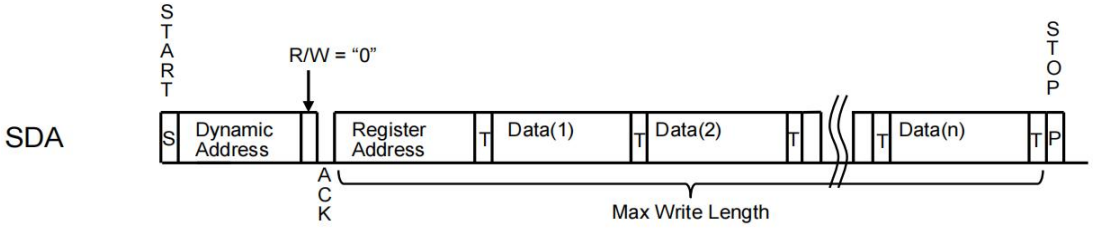


Figure 15, I3C Private WRITE

I3C SDR Read:

READ Instruction:

When the R/W bit is set to “1”, AS1560 performs read operation.

The read operation requires to execute WRITE instruction as dummy before a Slave Address for the READ instruction (R/W bit = “1”) is transmitted. In read operation, a START condition is first generated then a Dynamic Address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.

After AS1560 receives a T-Bit in response to this address transmission, a Repeated START condition and a Dynamic Address for the READ instruction (R/W bit = “1”) are generated again. AS1560 generates a T-Bit in response to this Dynamic Address transmission. Next, AS1560 transfers the data at the specified address then increments the internal address counter by one. If the Master generates a STOP condition instead of an acknowledge after data is transferred, the read operation stops.

Table 6, I3C Private READ Sequence

Master	Slave Device (AS1560)	Bus Condition
START Condition	Input at the start of communication	Open-Drain
7-bit Dynamic Address		Open-Drain
R/W=”0”	ACK (with Handoff)	Open-Drain
Access Address (1 Byte)	Parity Check, using T-Bit	Push-Pull
Repeated START Condition		Push-Pull
7-bit Dynamic Address		Push-Pull
R/W=”1”	ACK (without Handoff)	Push-Pull
Read Data (1 Byte)	T-Bit (with Handoff)	Push-Pull
Read Data (1 Byte)	T-Bit (with Handoff)	Push-Pull
|	|	|
STOP Condition	Input at the end of communication	Push-Pull

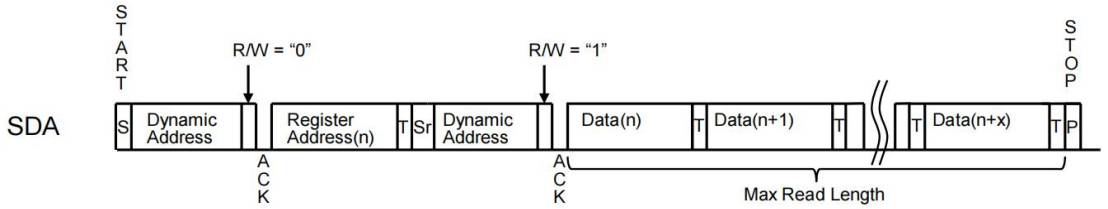


Figure 16, I3C Private READ

In-Band Interrupt (IBI):

AS1560 supports In-Band Interrupt (IBI) using the SDA line. The IBI can be used only in I3C SDR mode. After setting AS1560 to I3C SDR mode, set ***IBI_EN bit = “1”*** with the CCC (ENEC=0x80). The address of the interrupt control register is 0x20 ~ 0x22.

When IBI is enabled and each measurement mode is set, AS1560 starts magnetic measurement and monitoring of the I3C Bus. When the measurement is completed and it is determined that the bus is free, AS1560 drives the SDA line low and generates a START condition.

After AS1560 generates a START condition, AS1560 sends its own Dynamic Address and R/W bit = “1” in Open-Drain. AS1560 receives an acknowledgment from the Master and completes the IBI. If AS1560 fails to transmit its own address (another device drives SDA) and no acknowledgment is returned from the Master, wait for bus free status and perform IBI again. AS1560 repeats until IBI is completed.

IBI Payload consists of a single byte. The content is identical to that of Register ox10 STAT1.

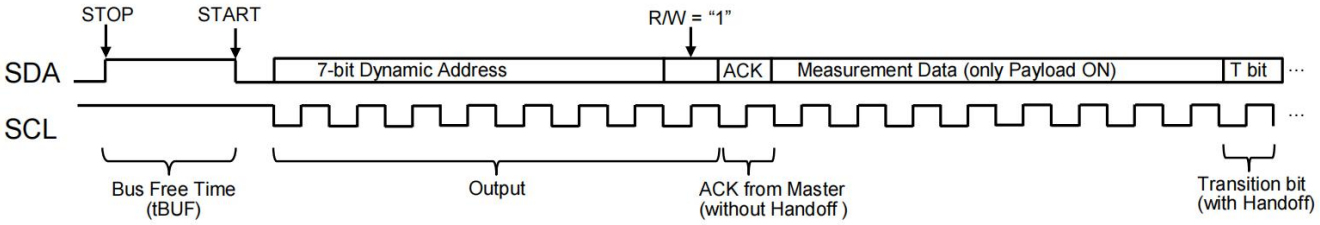


Figure 17, In-Band Interrupt Data Format

Command Code	Command Code	Broadcast /Direct	Set/Get	Brief Description
80h	ENEC	Direct	Set	Enable Events Command, “1” Enable
81h	DISEC	Direct	Set	Disable Events Command, “1” Disable

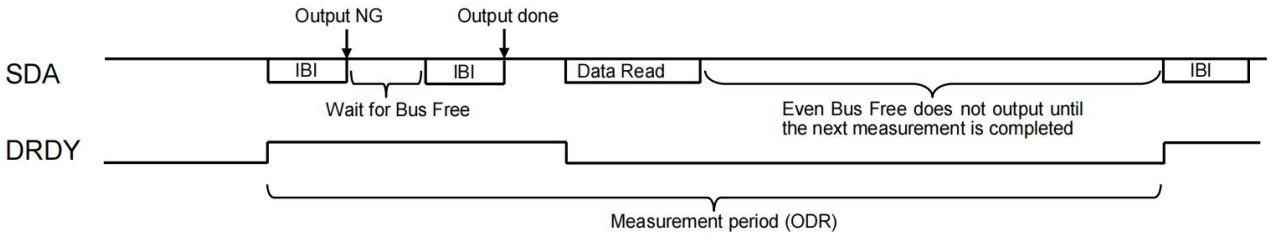


Figure 18, In-Band Interrupt Output Flow

Registers

Description of Registers:

AS1560 has registers of **17** addresses as indicated in Table 16. Every address consists of 8 bits data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 7, Register Table

Address	*Name*	*Mode*	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	INT_DELAY	*Write/Read*	Set the number of consecutive threshold events required to assert the INT pin.								10H
01H	INT_CONFIG	*Write/Read*	Configures interrupt enable, clear behavior, and trigger condition.								00H
02H	BOPL_LO	*Write/Read*	Low byte of the Operate Point Low Threshold.								00H
03H	BOPL_HI	*Write/Read*	High byte of the Operate Point Low Threshold.								00H
04H	BOPH_LO	*Write/Read*	Low byte of the Operate Point High Threshold.								00H
05H	BOPH_HI	*Write/Read*	High byte of the Operate Point High Threshold.								00H
06H	HYS	*Write/Read*	Set the Hystersis applied to the release point.								00H
07H	SRST	*Write/Read*	Software Reset, resets all registers to default values.								00H
08H	CNTL1	*Write/Read*	Configures operation mode and output data rate.								00H
09H	DID	*Read*	Device ID								83H
0DH	DR & RES	*Write/Read*	Set magnetic dynamic range and output resolution.								00H
0EH	MOV	*Write/Read*	Configures moving average filter strength.								00H
10H	STAT1	*Read*	Provides data ready and interrupt status flags.								80H
11H	DATAZL	*Read*	Low byte of the magnetic data.								00H
12H	DATAZH	*Read*	High byte of the magnetic data.								00H
6CH	AVER_Z	*Write/Read*	Defines the averaging count for magnetic measurement.								20H
71H	ADR_LOCK	*Write/Read*	Locks the I2C Address								00H

When VDD is turned on, POR function works and all registers of AS1560 are initialized regardless of VID status. To write data to, or read data from, register, VID must be on. TS1 and TS2 are test registers for shipment test. Do not access these registers.

Control 1: INT_DELAY Registers (R/W) (ADDR 0x00h, Default 10h):

INT_DELAY register controls the number of consecutive magnetic threshold events required to assert the INTB (Figure 8). This mechanism helps reduce false triggers caused by transient magnetic noise. The register also includes a bit to manually clear INTB when operating in latched mode.

INT_DELAY Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R	R	R	R/W
Value	0	0	0	1	0	0	0	0
Function	Interrupt_Delay[7:4]				Reserved[3:1]			Interrupt_Unlock

Interrupt_Delay[7:4]: default (1111h)

Number of consecutive valid threshold events required to assert INTB (High to Low). Valid range: 1 - 15 (0 is not used) . Default 1.

Interrupt _Unlock: default (0h)

Write 1 to manually clear INTB in Latch mode (Interrupt_Lock = 0). Must be cleared (set to 0) before re-enabling.

Control 2: INT_CONFIG Registers (R/W) (ADDR 0x01h, Default 00h):

This register defines the interrupt logic behavior. It allows enabling or disabling the interrupt function, configuring the latching behavior of INTB, and selecting the magnetic field condition that triggers the interrupt.

INT_CONFIG Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	INT_EN	Interrupt_lock	Reserved	INT_TYP	Reserved			

INT_EN: default (0h) Enables the interrupt function

0 = Disabled

1 = Enabled

Interrupt _lock: default (0h) Selects INTB clear behavior

0 = Latch Mode, INTB remains low until cleared via interrupt_unlock.

1 = Normal Mode (No Latch)

INT_TYP: default (0h) Defines interrupt trigger condition (Figure 7)

0 = INTB is active low when the field is outside the threshold window.

1 = INTB is active low when the field is within the threshold window.

Control 3-6: BOP/BRP Setting Registers (R/W) (ADDR 0x02h ~ 0x05h, All Default 00h):

The Device allows configuration of the magnetic operate and release thresholds used for interrupt generation. These thresholds — the low and high operate points (BOPL and BOPH) — define the magnetic field range in which interrupts are triggered. Each value is stored as a signed 16-bit value in two's complement format, allowing both positive and negative field levels to be set.

Rule: The values must be set within the constraints of the sensor's measurement capability:

-32767 < BOPL < BOPH < +32767

These registers define the lower and upper bounds of the threshold window:

BOPL_LO Register Byte (0x02h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	Low Operate Point Low Byte							

BOPL_HI Register Byte (0x03h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	Low Operate Point High Byte							

BOPH_LO Register Byte (0x04h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	High Operate Point Low Byte							

BOPH_HI Register Byte (0x05h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	High Operate Point High Byte							

Control 7: HYS Registers (R/W) (ADDR 0x06h, Default 00h):

Magnetic Switch Hysteresis: Controls the hysteresis amount for the release point (BRP). The value set in this register is multiplied by 4 to calculate the actual hysteresis value applied in the magnetic threshold logic.

HYS Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	HYS[7:0]							

Hys = 4* B_{HYS}

If INT_TYP=1: BRPL = BOPL - HYS; BRPH = BOPH + HYS;

If INT_TYP=0: BRPL = BOPL + HYS; BRPH = BOPH - HYS;

Control 8: SRST Registers (R/W) (ADDR 0x07h, Default 00h):

Software Reset Register: The Software Reset Register (SRST) provides a mechanism to reset AS1560 to its default state. This register is used to reset IC. (Please wait 20mS before any command after setting SRST="1").

SRST Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	Reserved							SRST

SRST: Software Reset Control default (0)

If you want to reset the IC, set SRST = "1".

When SRST = "1", all registers are initialized. After reset, SRST bit turns to "0" automatically.

Please wait 20ms before any command after setting SRST="1".

Control 9: CNTL1 Control Setting Registers (R/W) (ADDR 0x08h, Default 00h):

Control Setting Register 1 (CNTL1): configuring the operational mode and output data rate (ODR) of the AS1560 sensor. Controls and adjusts the main parameter set.

CNTL1 Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0
Function	CNTL1[7:0]							

CNTL1[7:0]: Configuring the Operational mode and output data Rate Setting default (00000)

CNTL1[7:0]	Description
00h	Stand-by mode (default)
10h	Continuous measurement mode with ODR 10Hz
20h	Continuous measurement mode with ODR 6.7Hz
30h	Continuous measurement mode with ODR 5Hz
40h	Continuous measurement mode with ODR 80Hz
50h	Continuous measurement mode with ODR 40Hz
60h	Continuous measurement mode with ODR 26.7Hz
70h	Continuous measurement mode with ODR 20Hz
80h	Single measurement mode
90h	Continuous measurement mode with ODR 100Hz
A0h	Continuous measurement mode with ODR 50Hz
B0h	Continuous measurement mode with ODR 1Hz
C0h	Continuous measurement mode with ODR 200Hz
D0h	Continuous measurement mode with ODR 250Hz
E0h	Continuous measurement mode with ODR 320Hz
F0h	Continuous measurement mode with ODR 500Hz
F8h	Continuous measurement mode with ODR 1KHz
E8h	Continuous measurement mode with ODR 2KHz
D8h	Continuous measurement mode with ODR 4KHz

When each mode is set, AS1560 transits to the set mode. Refer to ***Operation Mode*** for detailed information. If other value is set, AS1560 transits to Power-down mode automatically.

*** Special Considerations for High ODR Settings:***

For output data rates exceeding 1 kHz (settings 0xF8, 0xE8, 0xD8), it is crucial to maintain an I²C clock speed of 1 MHz to ensure that the read operations do not interfere with the data update times.

Control 10: Device ID Register (Read) (ADDR 0x09h, Default 83h):

DID Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R	R	R	R	R	R	R
Value	1	0	0	0	0	0	1	1
Function	DID[7:0]							

DID[7:0]: Device ID default (83h)

Device ID of AS1560. It is described in one byte and fixed value; 0x83H: fixed.

Control 11: Dynamic Range and Resolution Setting Registers (R/W) (ADDR 0x0Dh, Default 00h):

The Dynamic Range and Resolution (DR&RES) register allows users to customize the operating magnetic field range and the resolution of the magnetic sensor.

DR & RES Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Value	0	0	0	0	0	0	0	0
Function	DR[7:5]			ADC_RS[4:1]				Reserved

DR[7:5]: Dynamic Range Setting default (000) Configures the maximum measurable magnetic filed.

DR[7:5]	*Description*
000	±163.84mT
001	±81.92mT
010	±40.96mT

ADC_RS[4:1]: Sets the Resolution of the magnetic sensor default (0000)

ADC_RS[3:0]	*Description*	*ADC_RS[3:0]*	*Description*
0000	16-bits	0101	11-bits
0001	15-bits	0110	10-bits
0010	14-bits	0111	9-bits
0011	13-bits	1000	8-bits
0100	12-bits		

Control 12: Moving Average Setting Registers (R/W) (ADDR 0x0Eh, Default 00h):

The Moving Average (MOV) register is instrumental in managing signal noise through the application of moving average filtering. This feature helps smooth out data by averaging over a set number of samples, thus reducing random fluctuations, and enhancing measurement reliability.

MOV Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R	R/W	R/W	R	R	R	R
Value	0	0	0	0	0	0	0	0
Function	Reserved		MOV[5:4]		Reserved			

MOV[5:4]: Moving Average Weight Setting default (00) Controls the intensity of the moving average filter applied to the sensor data.

MOV[5:4]	*Description*
00	Disable moving average
01	Low
10	Middle
11	High

Control 13: Data State Registers (R) (ADDR 0x10h, Default 80h):

The Data State (STAT1) provides critical status information about AS1560's operational state and data integrity. This register is used primarily to check the readiness of the sensor data and to monitor for any data overrun conditions.

STAT1 Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R	R	R	R	R	R	R
Value	1	0	0	0	0	0	0	0
Function	INTM	Reserved				DORZ	Reserved	DRDY

INTM: default (1)

Mirrors the status of the PAD INTB (Interrupt Pin).

DORZ: Indicates if data has been skipped due to not being read before the next data update.

'0', No data overrun

'1', Data is overrun

Bit will release after sensor output data register read.

DRDY: Status for data ready. DRDY bit turns to "1" when measured data is ready to output.

'0', Not ready, normal

'1', Data is Ready, can be read from the sensor output data register.

Bit will release after sensor output data register read.

Control 14 - 15: Output Data Registers (R) (ADDR 0x11h ~ 0x12h, Default 00h):

The measurement output data store registers, which is represented in a 2's complement format.

DATAZL Register Byte (0x11h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R	R	R	R	R	R	R
Value	0	0	0	0	0	0	0	0
Function	Measurement Magnetic Low Byte Data							

DATAZH Register Byte (0x12h)								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R	R	R	R	R	R	R
Value	0	0	0	0	0	0	0	0
Function	Measurement Magnetic High Byte Data							

Control 16: Average Setting Registers (R/W) (ADDR 0x6Ch, Default 20h):

Control and adjusts main parameter set for sensor averaging.

AVER_Z Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R	R/W	R/W	R/W	R	R	R	R
Value	0	0	1	0	0	0	0	0
Function	Reserved	AVER_Z[6:4]			Reserved			

AVER_Z[6:4]: Average Count for Sensor

The control signal will repeat the number of averages.

AVER_Z[6:4]	*Repeat Number*	*AVER_Z[6:4]*	*Repeat Number*
000 (0)	256	100 (4)	32
001 (1)	4	101 (5)	64
010 (2)	8 (default)	110 (6)	128
011 (3)	16	111 (7)	256

Control 17: Address Lock Registers (R/W) (ADDR 0x71h, Default 00h):

Defines the setting for locking the address.

ADR_LOCKED Register Byte								
Byte	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	R/W	R	R	R	R	R	R	R
Value	0	0	0	0	0	0	0	0
Function	Address Lock	Reserved						

Typical Application Circuit

I2C Bus Interface:

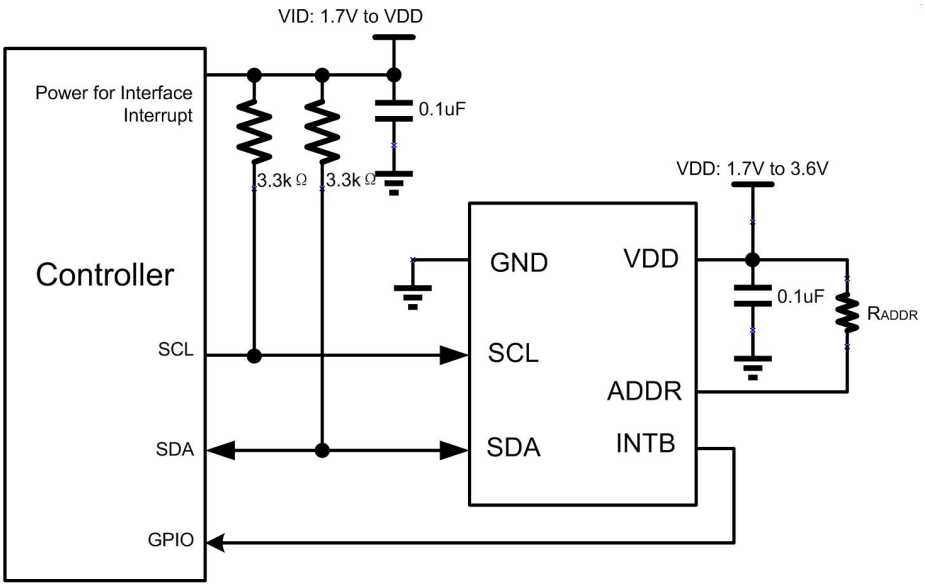


Figure 19, Typical I2C Bus Application Circuit of AS1560

Thermal Considerations:

For continuous operation, do not exceed the maximum operation junction temperature 150°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, TA is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of AS1560, the maximum junction temperature is 150°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WLCSP-6L package, the thermal resistance θ_{JA} is 185°C/W. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$$P_{D(MAX)} = \frac{(150^oC - 25^oC)}{185^oC/W} = 0.67W$$

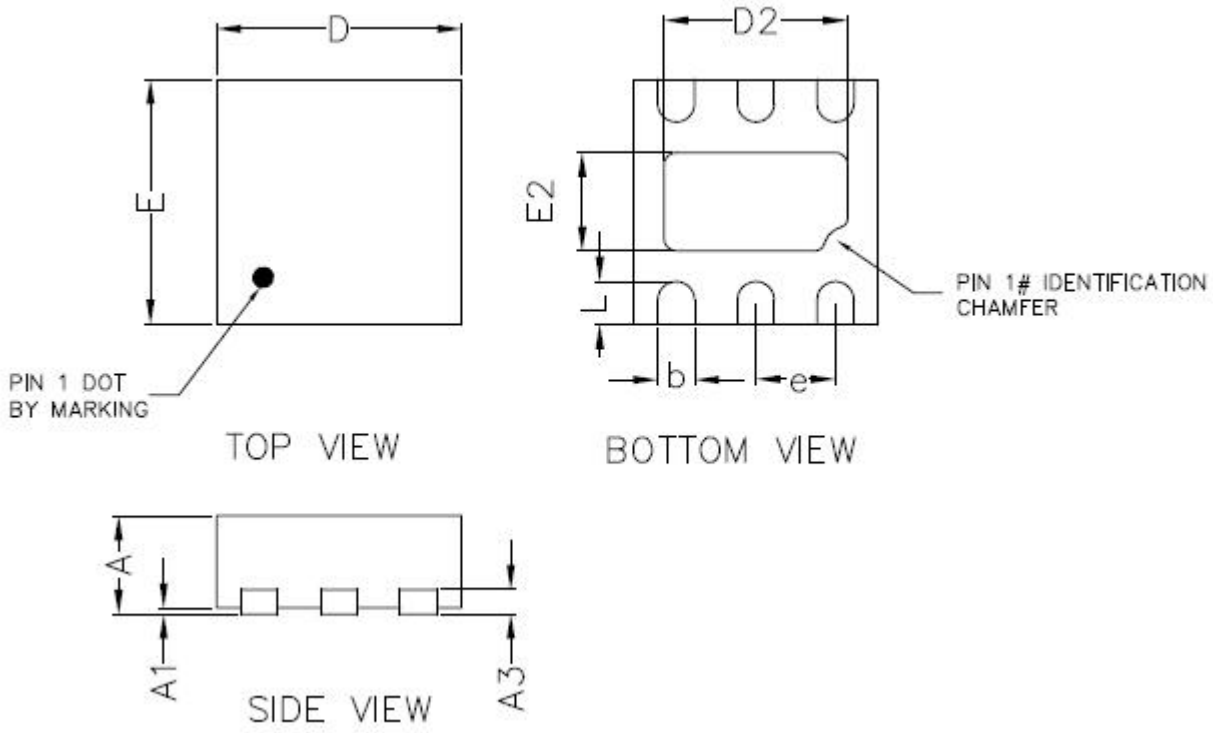
Layout Considerations

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the AS1560 the following PCB layout guidelines are recommended.

- Keep the power ground plane on the top layer (all capacitor grounds and PGND pins must be connected together with one uninterrupted ground plane).
- AND must be connected together on the same ground plane.
- Place the flying capacitor as close as possible to the IC.
- Always avoid vias when possible. They have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics especially for power lines.
- For high dv/dt signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For high di/dt signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Keep input capacitor close to the IC with low inductance traces.
- Keep trace from switching node pin to inductor short if possible: it reduces EMI emissions and noise that may couple into other portions of the converter.
- Isolate analog signal paths from power paths.

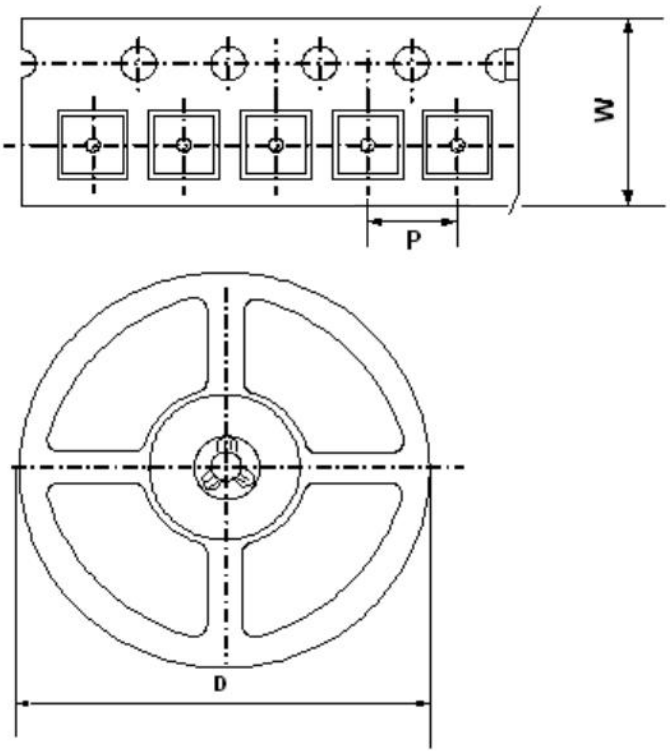
Package Information

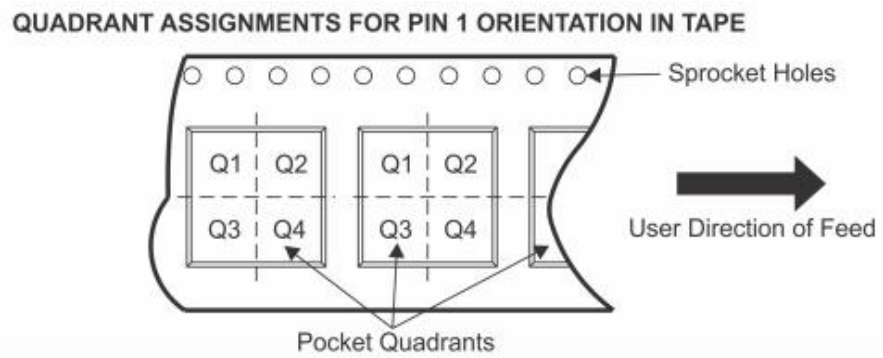
DFN2020-6L:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.027	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200 BSC		0.008 BSC	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D2	1.350	1.600	0.053	0.063
E2	0.650	0.900	0.026	0.035
b	0.200	0.350	0.008	0.014
e	0.650 BSC		0.026 BSC	
L	0.250	0.350	0.010	0.014

■ Packing Information





Device	Package Type	SPQ	Carrier Width (W)	Pitch(P)	Reel Size(D)	A1 Quadrant
AS1560DRN	DFN2020-6L	3000pcs	8.0±0.1 mm	4.0±0.1 mm	180±1 mm	Q1

Note: Carrier Tape Dimension, Reel Size and Packing Minimum

■ Revision History:

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision 0.1 (May 2026) to Revision 1.0 Page

- Using the test data and modify the electrical characteristics and fill in the Parameter..... 4
- Modify the packing information.....26

Changes from Original (March 2025) to Revision 0.1 Page

- Initial Release Specification .....